OPERATIONAL AMPLIFIER INTEGRATOR

The present invention relates to an operational amplifier (op amp) integrator.

It is known to construct integrator circuits from op amps by connecting a resistor to the input of a transistor circuit and using a capacitor as a feedback element. The ideal integrator has infinite gain and only a single pole when the frequency of the applied

5   signal is zero. However, practical integrator circuits based on a transconductance stage have a zero in the right halfplane when the frequency of the applied signal is equal to the feedback capacitance divided by the transconductance of the transistor.

It is an object of the present invention to provide an improved operational

10   amplifier integrator and particularly to compensate for the right halfplane zero.

According to the present invention there is provided

an integrator circuit comprising:

-    a transistor stage

-    a feedback capacitor connected between the input and the output of the transistor stage;

15   -   a resistor connected to the input of the transistor stage;

-    characterised by an additional circuit branch comprising:

-    a second capacitor and a second resistor connected in series one with the other and connected between the output of the transistor stage and the inverted input to the integrator circuit.

20   Preferably two additional circuit branches are provided: one may be connected between the positive input and output of the transistor stage and one connected between the negative input and output. This is particularly useful for balanced amplifier topology. The transistor is an invertor and thus positive input voltages provide negative output voltages and vice versa.

25   The invention finds particular application in the first filter stage (integrator) in a sigma delta analog to digital conversion circuit. This first filter stage is very hard to design.

The extra circuit branch 20 has a current I_3 and comprises a second capacitor 22 and a second resistor 25 connected in series between an inverted input voltage $-V_{in}$ and the non-inverting output node 3 of the transistor stage 1.

The equations 7 to 13 in figure 6 illustrate how the extra circuit branch 20 compensates for the zero in the right half plane.

Equation 7 is the same as Equation 1 in figure 5 and gives the value of the current I_2 in the feedback branch comprising capacitor 2. Equation 8 gives the current I_3 in the xtra circuit branch 20, and equation 9 sums these two currents.

In equation 10 the formula for the internal voltage V_+ in the transistor stage 1 is set out and this leads to equation 11, giving the current I_1 through the transistor stage 1.

Equation 12 assumes that the current in the three branches must cancel out, ie that the three currents add up to zero, and equation 13 then effectively sums the currents I_1, I_2 and I_3 given by equations 11, 7 and 8 respectively.

In equation 14 the terms are simplified to give an equation for the ratio of the output voltage to the input voltage. As can be seen from a comparison of equation 14 giving this ratio for the new circuit of figure 2, with the equation 6 giving the ratio for the known circuit of figure 1, the new circuit compensates for the zero in the right halfplane, and this compensation is not dependent on the characteristic of the amplifier.

Figure 3 illustrates an op amp integrator using balanced amplifier topology, which is well known to persons skilled in the art. The bias amplifier is a transconductance so that a positive input voltage leads to a current sink at the output and hence a negative voltage at the output. The circuit is essentially the same as that in figure 2 but the circuit elements are repeated on the other side of the transistor stage 31 essentially in mirror image. Thus a first input voltage V_{in} is connected via a first input resistor 35a to a first input terminal 34 of transistor stage 31. A first feedback capacitor 32a is connected between the first input terminal 34 and a first output terminal 33 at which a first output voltage V_{out} appears.

An negative input voltage $-V_{in}$ is connected via a second input resistor 35b to a second input terminal 36 of transistor stage 31. A second feedback capacitor 32b is connected between the second input terminal 36 and the second output terminal 37 at which a negative output voltage $-V_{out}$ appears.

Two extra circuit branches, each comprising a capacitor and a resistor in series, are provided. A first extra circuit branch 320a comprises a capacitor 322a and a resistor 325a. This connects the negative input voltage $-V_{in}$ to the first output terminal 33 at which the positive output voltage V_{out} appears. A second extra circuit branch 320b comprises

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a capacitor 322b and a resistor 325b. This connects the positive input voltage V_{in} to the output terminal 37 at which the negative output voltage $-V_{out}$ appears.

In figure 4 a circuit diagram is presented wherein the invention is applied to the first stage of a sigma delta analog to digital convertor. This circuit comprises the circuit elements shown in figure 3 and denoted by the same reference symbols and some additional resistors and output voltage lines. The additional resistors have a different value R2 to the resistors R1 shown in the previous figures. Each is connected between respective resistors R1 and capacitors C and an additional output voltage line. Thus resistor 41 connects resistor 325a to analog output voltage line 45 on which the positive analog voltage V_{DAC} appears. Resistor 42 connects input terminal 34 of transistor stage 31 to output line 45 (V_{DAC}).

Likewise resistor 43 connects resistor 325b to analog output voltage line 46 on which a negative analog voltage $-V_{DAC}$ appears. Resistor 44 connects input terminal 36 of transistor stage 31 to the inverting analog output line 46 ($-V_{DAC}$).